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An Improved Buck PFC Converter with High Power Factor

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Abstract: In This paper an improved buck power factor correction (PFC) converter topology is proposed in this paper. By adding an aux-iliary switch and two diodes, the dead zones in ac input current of traditional buck PFC converter can be eliminated. An improved constant ON-time control is proposed and utilized in this improved buck PFC converter to force it that operates in critical conduction mode (CRM).In this paper of voltage source and current wave form in by using MATLAB/SIMULINK

Keywords: Buck Power Factor Correction (PFC), critical conduction mode (CRM), zero voltage switching (ZVS).

I. INTRODUCTION

Nowadays, most ac/dc power converters are forced to reduce the harmonic current to meet the some special power products such as lighting equipments Power factor correction (PFC) is a good method for providing an almost sinusoidal input current. The boost converter is the most popular topology for PFC applications due to its in-herent current shaping ability [1]–[2]. However, with universal input, usually a 400 V_{dc} output voltage is required for the boost PFC. The boost PFC cannot achieve high efficiency at low line input because it works with large duty cycle in order to get high-voltage conversion gain. Therefore, it is hard to increase the power density of boost PFC converter due to the thermal concern at low line input. THE Sepic converter [3], [4] and quadratic buck-boost [5], [6] can achieve high power factor (PF) and reduce the output voltage stress. But the voltage stress of switch in these two topologies is much higher than that in the boost PFC converter that reduces the efficiency and increases the cost. In this paper, an improved buck PFC converter is proposed, as shown in Fig.1. Compared with the conventional buck PFC converter, an auxiliary switch and two diodes are added in the improved buck PFC converter. The proposed converter has two different operation modes in a line period. When the input voltage is higher than the output voltage, the proposed con-verter operates in buck mode, which is same as the conventional buck converter. When the input voltage is lower than the output voltage, the proposed converter operates in buck-boost mode The buck PFC converter has some attractive merits. First, the output voltage of buck converter is always regulated lower than the boost converter. Second, the voltage across the main switch of the buck converter is almost clamped to the input voltage. Therefore, the buck PFC converter can achieve relatively high efficiency within the universal input voltage range and it has drawn more and more attention in the past years [9How-ever, if the buck converter operates in hard switching mode, the switching loss especially at high input will be large, which deteriorates the merit of the buck converter . The buck dc–dc converter operating in critical continuous conduction mode (CRM) can eliminate the reverse recovery loss in diode and achieve zero voltage switching (ZVS) for the switch The constant ON-time (COT) control for CRM buck PFC con-verter is introduced in With COT control, the peak current in the switch is almost proportional to the input voltage, and then high PF can be achieved.

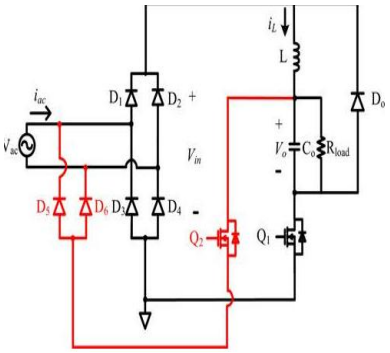

Fig. 1.Proposed improved buck PFC converter

II. P RINCIPLE OF OPERATION

In the proposed converter operates in CRM will be analysed in detail. To simplify the analysis, the transitions between the switches and the output diode D_o are omitted. After that, there still exist eight operation stages in a line period. Fig. 2 shows the equivalent circuits of the stages easy into it.

A. Positive Buck-Boost Operation Mode

When the input voltage V_{ac} is in positive half cycle and the magnitude of V_{ac} is smaller than V_o the proposed converter operates in buck-boost mode. During this mode, switch Q_1

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keeps OFF and switch Q_2 keeps switching. There are two stages when the proposed converter operates under this mode:

Stage 1: When switch Q_2 is ON, the proposed converter operates in stage 1. The equivalent circuit of this stage is shown in Fig. 2(a). The inductor L is charged by V_{ac} through D_1 and D_6 , and i_L increases during this stage

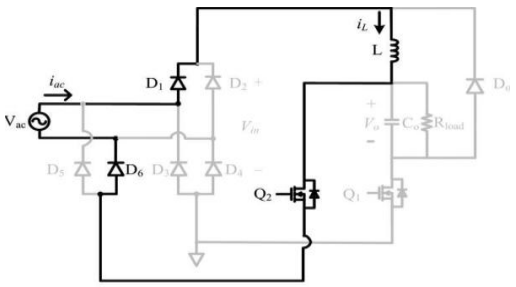

Fig:2(a) Equivalent circuits of the proposed converter in First stages

Stage 2: When switch Q_2 is OFF, the proposed converter operates in stage 2. The equivalent circuit of this stage is shown in Fig. 2(b). The inductor L is discharged by V_o through D_o , and i_L decreases during this stage

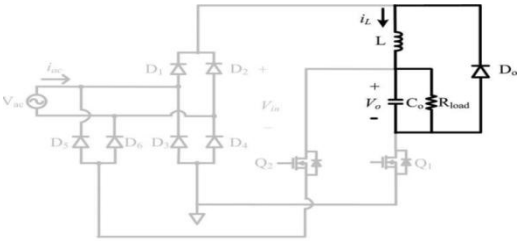

Fig:2(b) Equivalent circuits of the proposed converter in Second stages

B. Positive Buck Operation Mode

When the input voltage V_{ac} is in positive half cycle and the Magnitude is larger than V_o , the proposed converter operates in buck mode. During this mode, switch Q_2 keeps OFF and Switch Q_1 keeps switching There are two stages when the proposed converter operates under this mode:

Stage 3: When switch Q_1 is ON, the proposed converter operates in stage 3. The equivalent circuit of this stage is shown in Fig. 2(c). The inductor L is charged by $V_{ac} - V_o$through D_1 and D_4 , and i_L increases during this stage.

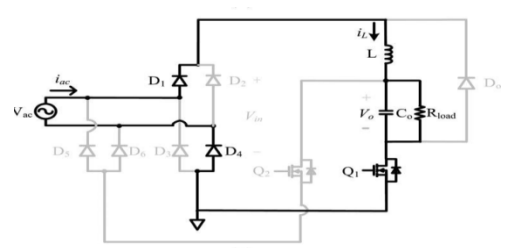

Fig:2(c) Equivalent circuits of the proposed converter in Third stages

Stage 4: When switch Q_1 is OFF, the proposed converter operates in stage 4. The equivalent circuit of this stage is same as that of stage 2, as shown in Fig. 2(b).

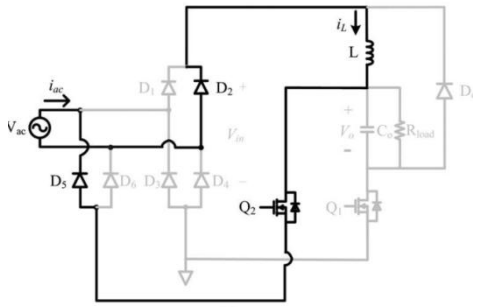

Fig:2(d) Equivalent circuits of the proposed converter in Five stages

The inductor L is discharged by V_o through D_o , and this section, the proposed converter operates in CRM will be analyzed in detail. To simplify the analysis, the transitions between the switches and the output diode D_o are omitted. After that, there still exist eight operation stages in a line period. Fig. 2 shows the equivalent circuits of the stagesbe separated into four operation stages defined as stages 5–8, and the equiv-alent circuits include Fig. 2(b), (d), and (e). The negative half cycle operation processes of the proposed converter are similar to those of the positive half cycle. For simplicity, the negative operation processes are not depicted in detail here

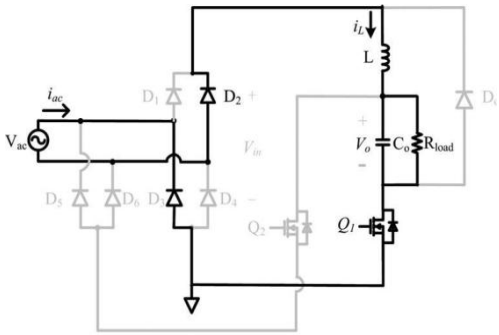

Fig:2(e) Equivalent circuits of the proposed converter in six stages

An improved COT control is applied for the proposed buck PFC converter to force it that operates in CRM, as shown in Fig. 3. The output voltage is detected with a level-shift cir-cuit formed by a high-voltage transistor Q_2 and the resistors $R_{a1} \sim R_{a4}$. Some key waveforms are shown in Fig. 4.As shown in Fig. 3, the control signal V_{ph} used to control the converter either in buck mode or buck-boost mode is achieved by comparing the detected V_{in} signal V^{-}_{in} with a voltage reference $V_{boundry}$. Usually, $V_{boundry}$ is set to reflect the output voltage V_o with the same ratio as that V^{-}_{in} reflects V_{in} . V_{ph} is high logic when V^{-}_{in} is higher than $V_{boundry}$ and is low logic when V^{-}_{in} is lower than $V_{boundry}$. The detected output signal V_{FB} is sent to the negative input of the error amplifier U_f . The error between V_{FB} and the set reference V_{ref} is amplified by the compensation networks C_f and an amplified error signal $V_{com\,p}$ is achieved. The dc voltage signal $V_{com^{-}\,p}$ applied to control the conduction period T_{ON} is achieved from $V_{com\,p}$ through a control networks formed by resistors R_1 and R_2 and switch S_1 . Switch S_1 is controlled by the control signal V_{ph} . The proposed converter operates in buck mode when

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S_1 is OFF and operates in buck-boost mode when S_1 is ON. V_{com^-p} is a step function controlled by V_{ph} , as shown in (1)

$$V'_{comp} = \begin{cases} V_{comp} & V_{in} > V_o \\ k \cdot V_{comp} & V_{in} \le V_o \end{cases} \quad (1)$$

III. SCHEMATIC OF THE PROPOSED BUCK PFC CONVERTER WITH AN IMPROVED COT

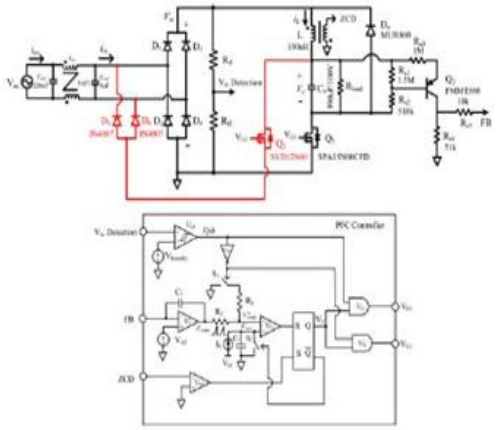

Fig. 3. Schematic of the proposed buck PFC converter with an improved COT control

This level transition sets the driving signal from low level to high level According to the aforementioned analysis; the rising slope of *V*saw is constant due to the constant current source *I*1 charging during the whole line period. Therefore, the ON-time (*T*ON) of the switches is determined by *V* _comp proportionally. Smaller value of *k* leads to smaller *T*ON and smaller peak values of *iL* when the proposed converter is operating in buck-boost mode As shown in Figs. 3 and 4, the driving signals *VG*1 and *VG*2 are controlled by *V*ph for the different operation modes alternately. Different coefficient *k* results in the different PF correction performance and the overall efficiency.

Where *k* is a coefficient equal to $R_1 /(R_1 + R_2)$. Similar to the conventional COT control, a constant current source I_1 , capacitor-tor C_1 , and switch S_2 are used to generate a saw tooth wave form V_{saw} . When V_{saw} reaches V_{com^-p} , the output of comparator $U_{c\ 1}$ jumps from low level to high level. This level transition results the driving signal from high level to low level.

The zero-crossing point of the inductor current i_L is detected by the auxiliary winding of the inductor *L*. This inductor current zero-crossing detection signal $V_{ZC\ D}$ can be applied in both buck and buck-boost modes. When the inductor current i_L falls to zero, the output voltage auxiliary winding $V_{ZC\ D}$ starts to fall. Once $V_{ZC\ D}$ falls to zero, the output of comparator $U_{c\ 2}$ jumps from low level to high level.

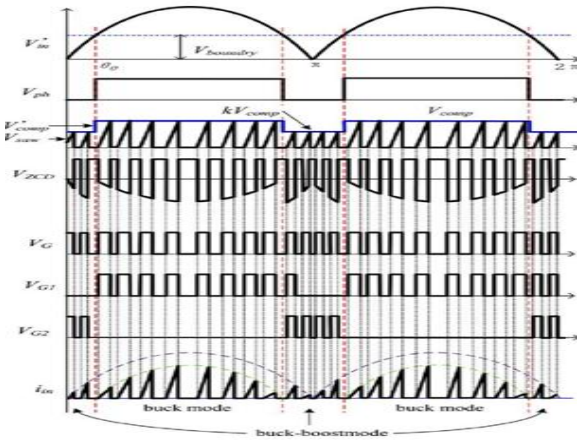

Fig. 4. Key waveforms in the improved COT control diagram.

IV. SIMULATION RESULTS

A. CONVENTIONAL CIRCUIT

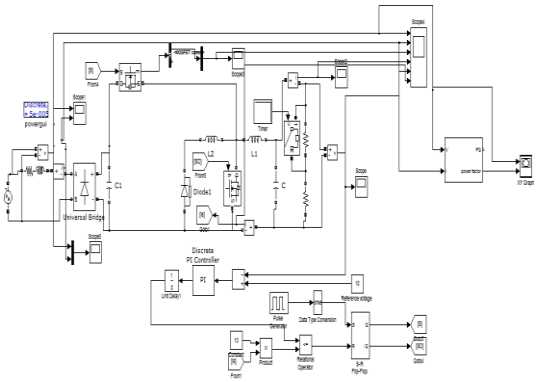

Fig 5. Conventional Circuit Buck PFC Converter with High Power Factor

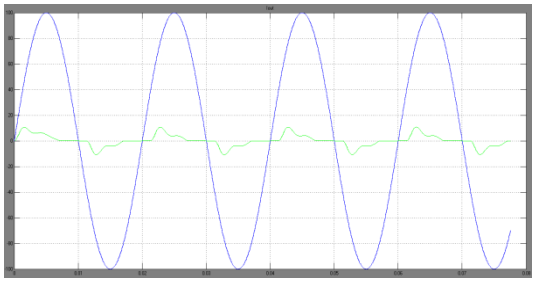

Fig6. Measured input voltage and input current waveforms of buck PFCconverter (100 Vac and full load).

B. PROPOSED CIRCUIT

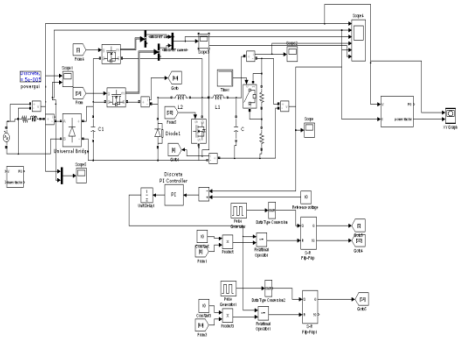

Fig **7.** Proposed Circuit Buck PFC Converter with High Power Factor

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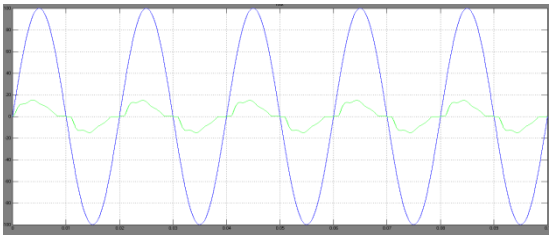

Fig 8.Measured input voltage and input current waveforms of the proposed converter (100 Vac and full load).

V. CONCLUSION

TThe improved buck PFC converter topology proposed in this paper is easy to achieve as the structure of the topology is simple. To operate in CRM, an improved COT control is proposed. The main disadvantage of this proposed topology is that two diodes and a switch are required and the added switch needs a floating driving circuit. However, the cost and size increase little compared to the whole cost and size. In conclusion, this proposed converter is very suitable for industrial application.

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